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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,235	DIEFFENDERFER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004 and 26 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *1,2,6 and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification as received on 24 March 2004; Claims as received on 24 March 2004; Abstract as received on 24 March 2004; Drawings as received on 24 March 2004; Oath and Declaration as received on 24 March 2004; IDS as received on 24 March 2004; Power of Attorney as received on 26 September 2006; and Assignee showing ownership per 37 CFR 3.73(b) as received on 26 September 2006.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 26 March 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

4. Claims 1, 2, 6, and 12-14 are objected to because of the following informalities:

   a. Claim 1: Please correct "said decode stage and instruction queue" in lines 5 and 7 to read --said decode stage and <u>said</u> instruction queue-- to clarify that the instruction queue referred to in the preamble is the instruction queue being referenced.

   b. Claim 2: Please correct "an instruction cache and said pipeline processor" in lines 1-2 to read --an instruction cache and [[said]]<u>an</u> pipeline processor-- or --[[an]]<u>said</u> instruction cache and said pipeline processor-- for consistency. Please

correct "said decode stage and instruction queue" in lines 5 and 7 to read --said decode stage and said instruction queue-- to clarify that the instruction queue referred to in the preamble is the instruction queue being referenced. Please correct "contents of an instruction queue" to read -- contents of [[an]]said instruction queue-- to clarify that the language is referring to the previously established instruction queue.

c. Claim 6: Please correct "loading said instruction from said cache memory in said decode stage" to read -- loading said instructions from said cache memory into said decode stage-- for consistency and clarification.

d. Claim 12: Please correct "said queue" in line 11 to read --said instruction queue-- for clarity. Please correct "from either from said decoder stage or from said cache" to read --from either[[from]] said decoder stage or [[from]]said instruction cache-- or --[[from]]either from said decoder stage or from said instruction cache-- for clarity.

e. Claim 13: Please correct "said queue" in line 3 to read --said instruction queue-- for clarity.

f. Claim 14: Please correct "said queue" in line 1 to read --said instruction queue-- for clarity.

5. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2, 4, 6, 8-10, and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claim 2 recites the limitations "said fetched instruction addresses" in line 6; "said instruction" in lines 6 and 8; and "the contents of an instruction queue" in line 12. There is insufficient antecedent basis for this limitation in the claim. There is no previous reference to a fetched instruction address in the claim or contents of the instruction queue. It is unclear what "said instruction" is referring to since "a plurality of instructions" and a branch instruction have been established. Is the language referring to an instruction in the plurality of instructions or the branch instruction?

9. Claim 4 recites the limitation "said instruction" in line 2. There is insufficient antecedent basis for this limitation in the claim. It is unclear what "said instruction" is referring to since "a plurality of instructions" and a branch instruction have been established. Is the language referring to an instruction in the plurality of instructions or the branch instruction?

10. Claim 6 recites the limitations "fetching the addresses of instructions" in line 2 and "said instruction queue instructions" in line 9. There is insufficient antecedent basis for this limitation in the claim. The claim has not previously established addresses of instructions or instruction queue instructions. It is unclear what are being referred to in these limitations.

11. Claims 8 and 9 recites the limitation "said instruction" in lines 2 and 3 of claim 8 and lines 3 and 5 of claim 9. There is insufficient antecedent basis for this limitation in the claim. The claims previously establish multiple instructions, but not an individual instruction.

12. Claim 10 recites the limitations "the contents of a location" in line 3, "the state of a valid bit" in line 4, and "said locations" in line 4. There is insufficient antecedent basis for this limitation in the claim.

13. Claim 13 recites the limitations "the contents of an instruction queue" in line 2. There is insufficient antecedent basis for this limitation in the claim. There is no previous reference to contents of the instruction queue.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1-8 and 10-14 are rejected under 35 U.S.C. 102(b) as being taught by Joshi et al., U.S. Patent Number 5,954,815 (herein referred to as Joshi).

16. Regarding claim 1, Joshi has taught a method for decreasing the latency between an instruction cache and a pipeline processor having a plurality of parallel execution stages, each execution stage having a decode stage and an instruction queue for sequentially processing instructions being processed by said processor, comprising:

a. Determining whether said decode stage and instruction queue do not have valid data (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

b. Inserting instructions from said instruction cache in parallel to said decode stage and instruction queue when said decode stage and instruction queue contain invalid data (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

17. Regarding claim 2, Joshi has taught a method for decreasing the latency between an instruction cache and said pipeline processor according to claim 1 further comprising:

a. Processing said cache instructions from said cache sequentially through said decode stage and instruction queue when valid data exists in said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

18. Regarding claim 3, Joshi has taught a method for processing instructions in a pipelined processor having a series of pipelined stages which reduces latency between an instruction queue and a pipeline processor comprising:

a. Serially fetching a plurality of instructions to be executed in said pipeline processor from a cache memory (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

b. Decoding each of said fetched instruction addresses in a first stage of said pipeline processor to determine if an execution branch is to be taken (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4,

line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

c. Loading said instruction into said instruction queue at the same time said instruction is being loaded in said decoder when said instruction queue and decoder are empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

d. Sequentially loading said instruction into ~aid instruction queue from said decoder when said instruction queue and said decoder are not empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

e. Shifting the contents of an instruction queue to produce an instruction from said instruction queue for processing in subsequent pipeline stages (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

19. Regarding claim 4, Joshi has taught the method for processing instructions in a pipelined processor according to claim 3 wherein said decoder identifies said instructions loaded in said queue at the same time as said instructions which are loaded in said decoder as valid or invalid during a subsequent cycle of said pipeline processor if an execution branch is not taken (Joshi

Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

20. Regarding claim 5, Joshi has taught the method for processing instructions in a pipelined processor according to claim 3 wherein said instruction queue contents are shifted left to an output port connected to plural pipelined processor stages (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7). In regards to Joshi, the contents of the queue are shifted from ibuf0 to ibuf1 to ibuf2, etc., as shown in Figure 3. The shift is relative to the position of the buffer, so it could be left or right. It does not matter, the operation would remain the same.

21. Regarding claim 6, Joshi has taught a method for executing instructions in a pipelined processor comprising: sequentially fetching the addresses of instructions to be executed by said pipelined processor;

a. Determining if said instructions are stored in a cache memory (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

b. Determining whether a decode stage and location of an instruction queue stage of said pipe line processor is empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

c. Loading said instruction from said cache memory in said decode stage and said instruction queue in parallel when said stages are empty (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

d. Sequentially reading out said instruction queue instructions for execution in said pipelined processor (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

22. Regarding claim 7, Joshi has taught the method for executing instructions in a pipelined processor according to claim 6 further comprising:

a. Loading only said decode stage with said instructions when said instruction queue contains valid data, and sequentially transferring said instructions to said instruction queue when a position in said instruction queue is available (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

23. Regarding claim 8, Joshi has taught the method for executing instructions in a pipelined processor according to claim 7 further comprising

a. Identifying said instruction as a branch instruction if said decoder predicts that a branch is being taken from said instruction (Joshi Abstract; column 2, lines 1-53;

column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

b. Inhibiting transfer of subsequent instructions from said decoder to said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7). In regards to Joshi, instructions are fetched from the predicted target, so the subsequent instructions directly following the branch are not fetched, i.e. inhibited from transfer to the decoder.

24. Regarding claim 10, Joshi has taught the method for executing instructions in a pipeline processor according to claim 6 further comprising:

a. Examining the contents of a location in said queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

b. Determining the state of a valid bit in each of said locations whereby the determination of whether said location contains valid data is made (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

25. Regarding claim 11, Joshi has taught the method for executing instructions in a pipeline processor according to claim 7, wherein said instructions are transferred from said decode stage to said instruction queue each time an instruction is read from said instruction queue (Joshi

Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

26. Regarding claim 12, Joshi has taught An apparatus for reducing the latency between stages of a pipelined processor comprising:

a. An instruction cache producing a plurality of instructions for execution by said pipelined processor (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

b. A plurality of decode stages connected to receive a plurality of instructions from said cache (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7);

c. An instruction queue having a plurality of locations for receiving an instruction and a valid bit (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7); and

d. A plurality of multiplexers for receiving each of said instructions, an output of a respective decode stage receiving said instructions, and connected to receive a valid bit from a location of said queue as a select signal, said multiplexer connected to supply each of said instruction queue locations with one of said instructions selected from either from said decoder stage or from said cache (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4,

line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

27. Regarding claim 13, Joshi has taught the apparatus according to claim 12, wherein said multiplexer receives a shift signal for said instruction queue which shifts the contents of said instruction queue towards an output port of said queue, and which enables said instructions from said decoder to be transferred to said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

28. Regarding claim 14, Joshi has taught the apparatus according to claim 12 wherein said output port of said queue is connected to a plurality of parallel processing stages (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

29. Regarding claim 14, Joshi has taught the apparatus according to claim 14 wherein said processing stages execute instructions belonging to one of a load/store operation, arithmetic operation, or a branch target instruction (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al., U.S. Patent Number 5,954,815 (herein referred to as Joshi), as applied to claim 7 above, in view of Free On-Line Dictionary of Computer (herein referred to as FOLDOC). Joshi has taught the method for executing instructions in a pipeline processor according to claim 7 further comprising forwarding said instruction to said decode stage for sequential transfer to said instruction queue (Joshi Abstract; column 2, lines 1-53; column 3, line 66 to column 4, line 34; column 4, line 51to column 5, line 16; column 6, line 35 to column 7, line 33; Figure 2A; Figure 3; and Figure 7). Joshi has not taught fetching an instruction from a main memory when said instruction is not in said cache memory. FOLDOC has taught an instruction from a main memory when said instruction is not in said cache memory (FOLDOC term "cache miss" ©1997). Joshi has taught that the instructions are fetched from the instruction cache (Joshi column 4, lines 1-4 and Figure 3), but has not taught where the instruction is fetched from when the cache does not contain the instruction. FOLDOC has taught that, when there is a cache miss, i.e. data cannot be found in a cache, the data is fetched from main memory (FOLD term "cache miss" ©1997). A person of ordinary skill in the art at the time the invention was made would have recognized that fetching data from main memory when it is not in the cache is necessary for execution to proceed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the cache miss of FOLDOC in the device of Joshi to ensure execution continues.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of

claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Satou et al., U.S. Patent Number 5,717,946, has taught handling branch instructions in an instruction queue system.

b. Matsuo, U.S. Patent Number 6,112,289 and 6,178,492, has taught a multiple instruction queue system for handling branch instructions.

c. Joshi et al., U.S. Patent Number 6,247,124, has taught an instruction queue system handling branch instructions.

d. Lynch et al., U.S. Patent Number 5,878,252 and 6,016,532, has taught a cache bypass system that fills both the cache and forwards the data to the execution unit when a cache miss occurs.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
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28 September 2006

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